

REMARKS

Claims 1-10 are pending in this application. Claims 1, 5, 9 and 10 are independent. Claims 9 and 10 are new.

Claim Rejection – 35 USC 103

Claims 1-8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art (e.g., Figures 1-6) in view of Tamai et al. (U.S. Patent 6,160,533, issued December 12, 2000, hereinafter Tamai). Applicant respectfully traverses this rejection.

Overcoming Tamai as 102(a) reference

A certified translation of the priority document (Japanese Patent Application No. 2000-299844) of September 29, 2000 is submitted herewith. Accordingly based on the date of the priority document, the Tamai patent is disqualified as prior art under 35 U.S.C. 102(a).

Disqualifying Tamai under 35 USC 103(c) via 102(e)

In addition, Applicant directs the Examiner's attention to M.P.E.P. 706.02(l)(1) which describes 35 U.S.C. 103(c). Based on 35 U.S.C. 103(c), subject matter which was prior art under former 35 U.S.C. 103 via 35 U.S.C. 102(e) is now disqualified as prior art if the subject matter and the claimed invention, were at the time the invention was made subject to an obligation of assignment to the same person.

The present application was filed after November 29, 1999, and both the present claimed invention (according to the assignment recorded August 30, 2001) and the Tamai patent are assigned

to Sharp Kabushiki Kaisha. Given that a certified translation of the priority document has been filed herewith resulting in Tamai qualifying as prior art only under 35 U.S.C. 102(e), Applicant submits that Tamai is disqualified as prior art based on the provisions of 35 U.S.C. 103(c), and respectfully requests that the rejection be withdrawn.

New Claims

Claims 9 and 10 have been added. Applicant submits that no new matter has been added. Claim 9 recites the combination of the Gamma resistance type voltage generation circuit based driver and the comparison type judgment circuit. Applicant submits that the prior art of record fails to teach this combination.

New claim 10 is directed to a method counterpart of claim 9. New claim 9 includes the feature of changing settings for every gradation output voltage level. Applicant submits that the prior art of record fails to teach this method counterpart of claim 9.

CONCLUSION

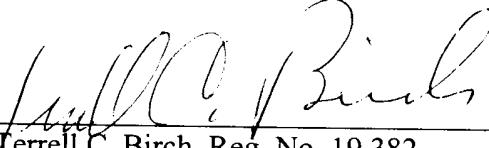
In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-10 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment:

Certified translation of priority document (Japanese Patent Application No. 2000-299844)